(Please write your Exam Roll No.)

Exam Roll No. _____

END-TERM EXAMINATION

THIRD SEMESTER [B.TECH.] DECEMBER-2008

Paper Code: ETCS/ETIC203
Paper Id : 27203/30203

Subject: Analog Electronics (Batch:2004-2007)

Maximum Marks : 75

Time : 3 Hours

Note : Attempt all questions including Q.1 which is compulsory. Internal choice is indicated.

Q.1 Answer the following

(a) Draw the energy level diagrams of intrinsic, P type and N type semiconductors. (1.5)

(b) Why is a schottky diode, and not an ordinary PN junction diode, considered suitable for rectification at high frequencies? (2)

(c) What is the difference between the forward voltage drops in case of germanium, silicon and light emitting diodes? (1.5)

(d) Give the Eber-Moll's model of a PNP transistor along with the equations for I_E and I_C. (2)

(e) Why is self bias preferred to fixed bias in a BJT amplifier circuits? (2)

(f) α of a BJT changes from 0.98 to 0.985. Find the percentage change in β. (2)

(g) Draw the circuit diagram of an R-C coupled amplifier. Draw its frequency response. (3)

(h) List the characteristics of an ideal operational amplifier. (3)

(i) Why is a field effect transistor called a voltage controlled diode? (1)

(j) Define the parameters of a field effect transistor and give the relationship between them. (2)

(k) Explain the difference between 'clipping' and 'clamping' circuits given an example of each. (3)

(l) What are the special features of an instrumentation amplifier? Also mention its typical application. (2)

Q.2 (a) Explain the difference between 'transition' and 'diffusion' capacitances of a PN junction diode. (3)

(b) Give the comparison between half wave and full wave rectifier circuits. (3)

(c) Sketch the output voltage wave form and find the DC voltage in the circuit shown in fig.1. (6.5)

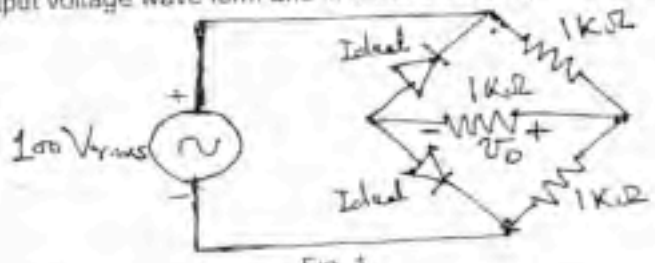


Fig. 1

OR

(a) Sketch the V-I characteristic of an ideal zener diode. (1)

(b) Explain the difference between 'Zener breakdown' and 'Avalanche multiplication'. (4)

(c) (i) The avalanche diode shown in fig.2 regulates at 50V over a range of diode currents from 5 to 40 MA. The supply voltage V=200V. Calculate R to allow voltage regulation from a load current I_L=0 uplo I_{max}? (4.5)

(ii) If R is set as in part (i) and the load current is set at I_L=25mA, what are the limits between which V may vary without loss of regulation in the circuit? (3)

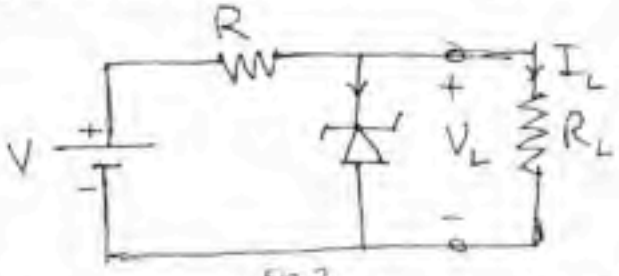


Fig. 2

Q.3 (a) Give an experimental setup to plot the output characteristics of an NPN transistor in CE configuration. (2)

(b) Sketch the typical output characteristics and indicate the various regions of operation. (2)

(c) Why is the slope of the CE output characteristics more than CB output characteristics? (3.5)

(d) For the circuit shown in fig. 3 find the following (5)

(i) Region of operation

(ii) V_0

Assume standard data for a silicon transistor.

P.T.O.

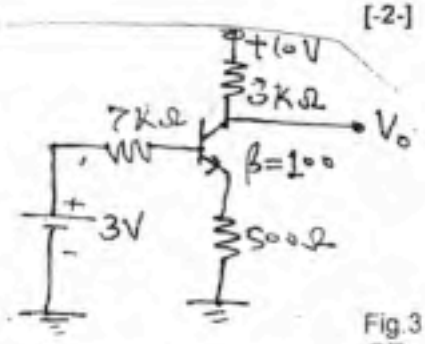


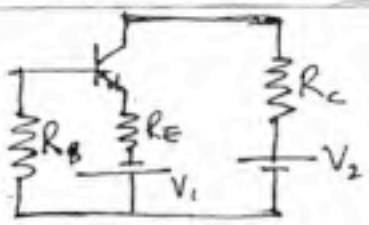
Fig.3

OR

(a) Explain the difference between dc and ac load lines with an example. **(3)**

(b) List and explain the factors responsible for Q point shift in BJT amplifier circuits. **(5)**

(c) For the two battery transistor circuit shown in fig.4 prove that the stability factor S is given by **(4.5)**



$$S = \frac{\beta+1}{1+\beta R_E/(R_E+R_B)}$$

Fig.4

Q.4 (a) Using h parameter model of a BJT derive general expressions for the following: **(8)**

(i) Input impedance
(ii) Current gain
(iii) Voltage gain
(iv) Output impedance

(b) For the transistor circuit shown in fig.5, the h parameters of the transistor are:

h_{ie}= 1500Ω h_{fe}= 100

h_{re}= 4 X 10^{-4} h_{oe}= 4 X 10^{-4}mho

Find the input impedance and the voltage gain of the amplifier. State clearly the assumptions made **(4.5)**

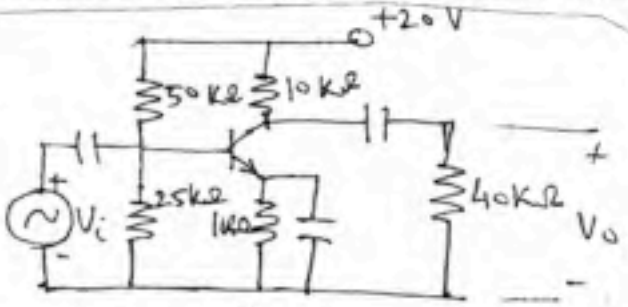


Fig.5

Q.5 (a) With reference to an operational amplifier explain the terms 'Input offset voltage' and 'slew rate'. **(4)**

(b) What is a precision rectifier? Explain with circuit diagram the use of an OP-Amp as a precision half wave rectifier. **(4.5)**

(c) Find V_o in the circuit shown in fig. 6 **(4)**

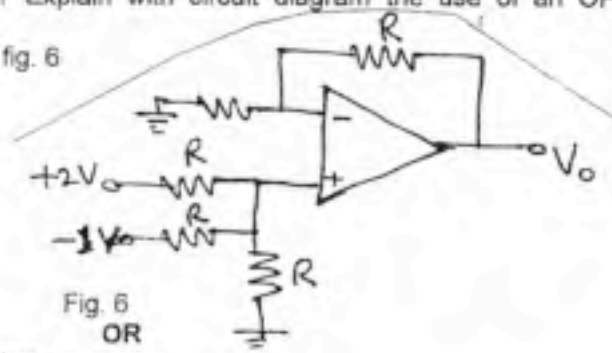


Fig. 6

OR

Write short notes on the following:

(i) Tunnel diode **(4)**

(ii) FET Biasing **(4)**

(iii) Active filters **(4.5)**

****