(Please write your roll no. immediately .....)

FIRST TERM EXAMINATION

III[rd] Semester [B. Tech.] | September'2008
Paper Code: ETEC-207 | Sub: Analog Electronics- I
Time: 1½ Hrs. | Max. Marks: 30

Note: Attempt Q. No. 1 and any two more questions.

Q. 1 (a) Prove that the depletion width W is proportional to the square root of total junction voltage in a reverse biased junction diode. (3)

(b) Draw the Ebers Moll model of a PNP transistor. Obtain equations for I_C & I_E (3)

(c) Explain the Early effect in transistors. (2)

(d) Explain the temperature dependence of V/I characteristics of a diode. (2)

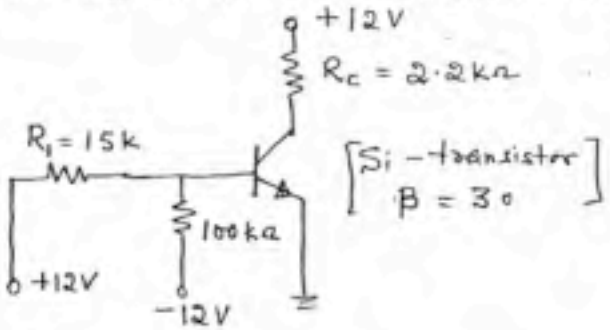
Q. 2 (a) Explain the switching behavior of a P-N junction diode when the input voltage changes from + V_F to $-V_R$. Discuss how storage time can be reduced. (5)

(b) Design a zener voltage regulator that will maintain an output voltage of 20 V across 1 kΩ load, when the input voltage range in 30-50 V. Determine R_S & maximum zener voltage.

Q. 3 (a) A half wave rectifier, having a load of 1 KΩ, rectifies an alternating voltage of 325 V peak value & the diode has a forward resistance of 100 Ω. Calculate (a) Average value of current. (b) D. C. power output, (c) Efficiency of the rectifier. (3)

(b) Write a short note on LED. (2)

(c) Determine the region of operation for the circuit shown. Assume typical values (5)



Q. 4 (a) Explain the saturation and cut off condition in a CE connected transistor. (5)

(b) The voltage at emitter, V_E = -5 V, V_{BE} = 0.7 V, find V_B, V_C, α , β for the circuit shown. (5)