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END TERM EXAMINATION

THIRD SEMESTER [B.TECH.]– DECEMBER 2008

Paper Code:ETEE203
Paper ID: 29203
Subject: Analog Electronics-I (Batch: 2004-2007)
Time : 3 Hours **Maximum Marks :75**

Note: Attempt five questions in all including Q.1 which is compulsory.

Q.1 Answer the following: - **(2.5x10=25)**

(a) Discuss the effect of temperature on the V-I characteristics of a pn-junction diode.
(b) Explain the difference in metals, semiconductors and insulators with the help of energy band diagram.
(c) Define α, β and I_{CBO} and I_{CEO}.
(d) Explain how cut-off condition is achieved in a transistor.
(e) An emitter follower is used as a buffer. Explain.
(f) Explain why voltage gain is stabilized in a CE amplifier if a resistance R_E is placed in the emitter branch.
(g) Explain 'Base Width Modulation'.
(h) Discuss the advantages of negative feedback in amplifiers.
(i) Show that the gain falls-off at the rate of 6dB/octave, in an RC-coupled amplifier.
(j) Give the advantages of FET over BJT.

UNIT-I

Q.2 (a) Explain the storage time effects in a pn-jn diode if the voltage applied to a diode is changed from $+V_F$ to $-V_R$. **(6)**

(b) In the circuit shown in Fig.1, the silicon diode has $V_\gamma = 0.6V$, $R_F = 10\Omega$, determine (i) the total voltage across R_L, (ii) the total current, i_D. **(6.5)**

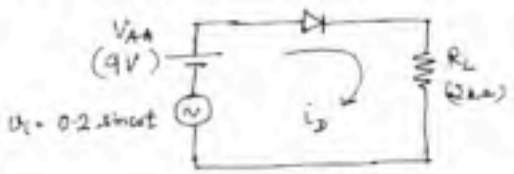

Fig. 1.

OR

Q.3 (a) For a step graded pn junction, prove that the transition capacitance, C_T is given by

$$C_T = A\left[\frac{q\varepsilon N_D}{2V_j}\right]^{\frac{1}{2}} ; \text{for } N_A >> N_D$$ **(6)**

(b) A 9V zener is used in the circuit shown in Fig.2. The load current is to vary from 12 to 100 mA. Find the value of the series resistor R and $I_{Z(max)}$. The input voltage is constant at 20V and $I_{Z(min)}$ = 10mA. **(6.5)**

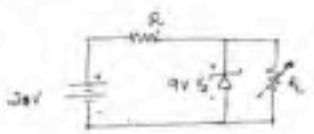

Fig. 2.

UNIT-II

Q.4 (a) Show the various regions of operation on the output characteristics of a transistor in CE configuration. Explain the shape of the curves quantitatively. **(6)**

(b) Analyse the circuit shown in Fig.3 to find the region of operation. Assume β_F = 100, $V_{BE,active}$ = 0.7V; $V_{BE,sat}$ = 0.8V, $V_{CE,sat}$ = 0.2V. **(6.5)**

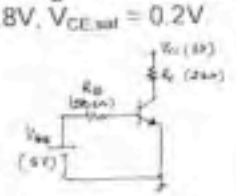

Fig. 3.

P.T.O.

OR

Q.5 (a) Prove that a self-bias circuit is better than a fixed bias circuit. **(6)**

(b) For the circuit shown in Fig.4, a silicon transistor with $\beta = 50$ at 25°C is used. It is desired that $V_{CE} = 5V$. Determine (i) R_B, (ii) the stability factor $S(I_{CO})$ (iii) the value of I_C at 100°C, if $\Delta I_{CO} = 19.9mA$. **(6.5)**

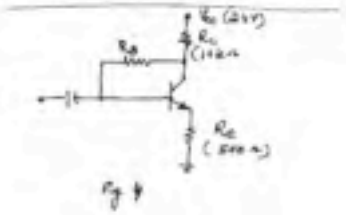

Fig 4

UNIT-III

Q.6 (a) Prove that : $h_{ic} = h_{ie}$; $h_{rc} = 1$

$h_{fc} = -(1+h_{fe})$; $h_{oc} = h_{oe}$ **(6)**

(b) The transistor in the amplifier shown in Fig.5 has the following parameters: $h_{ie} = 2K\Omega$; $h_{fe} = 50$; $h_{re} = 2 \times 10^{-4}$; $h_{oe} = 20 \times 10^{-6} A/V$. Determine: A_i; A_{vs}, R_i and R_o. Given $\beta = 200$. **(6.5)**

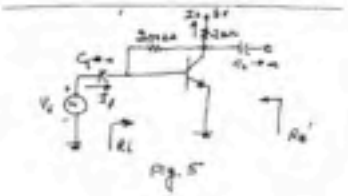

Fig. 5

OR

Q.7 (a) Explain the various components in a Hybrid-π model of a transistor at high frequencies. Define f_β & f_T and find the relation in these parameters. **(6)**

(b) A two stage amplifier is shown in Fig.6. Both the transistors are identical and have the parameters: $h_{fe} = 100$ and $h_{ie} = 1k\Omega$, $h_{oe} = 0$, $h_{re} = 0$. Determine the overall voltage gain. **(6.5)**

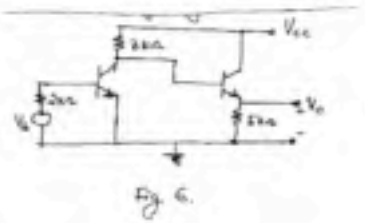

Fig. 6.

UNIT-IV

Q.8 (a) Explain the effect of negative feedback on the input and output impedances of an amplifier using voltage series feedback. Derive the generalized expression. **(6)**

(b) Explain the construction, drain and transfer characteristic of n-channel enhancement and depletion-type of MOSFETs. **(6.5)**

OR

Q.9 (a) Discuss the various advantages of negative feedback in amplifiers. Draw a circuit that uses (i) voltage shunt feedback (ii) current series feedback. **(6.5)**

(b) Explain (i) fixed-bias (ii) self-bias arrangement for biasing a JFET. **(6)**

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